Advanced Computer Architecture

Trial Examination: Multiple Choice

Time: 45 minutes

Questions: 22

At least one answer is correct.
Multiple Choice

1. To which class of systems does the von Neumann computer belong?
   a) SIMD (Single Instruction Multiple Data)
   b) MIMD (Multiple Instruction Multiple Data)
   c) MISD (Multiple Instruction Single Data)
   d) SISD (Single Instruction Single Data)
   e) None of the answers above is correct.

2. Parallel programs: Which speedup could be achieved according to Amdahl’s law for infinite number of processors if 5% of a program is sequential and the remaining part is ideally parallel?
   a) Infinite speedup
   b) 5
   c) 20
   d) 50
   e) None of the answers above is correct.
3. Instruction pipelining: After which total execution time is the result of the second task entering the pipe above ready?

a) 38 ns  
b) 33 ns  
c) 36 ns  
d) 37 ns  
e) None of the answers above is correct.
Multiple Choice

4. Standard CISC processor, no pipelining (around 1970): A vector operation $vc = va + vb$ with 5 elements per vector shall be performed. How many cycles are required within the loop below for the vector operation above (neglect the branch operation $br.less$) if the load instructions take two cycles and the remaining operations take 1 cycle?

a) 30
b) 35
c) 40
d) 45
e) None of the answers above is correct.

Standard scalar CISC processor:

- load $r2$=addr(va)
- load $r3$=addr(vb)
- load $r4$=addr(vc)
- load $r1$=0

loop:

- load $f1$=[r1+r2]
- load $f2$=[r1+r3]
- add $f3$=$f1$+$f2$
- store $[r1+r4]=f3$
- add $r1$=$r1+8$
- cmp $r1$, $(n*8)$
- $br.less$ loop

Cycles = ?
Multiple Choice

5. Standard RISC processor, with pipelining: A vector operation $vc = va + vb$ with 5 elements per vector shall be performed. How many cycles are required within the loop below for the vector operation above (neglect the branch operation `br.less`) if the load instructions take two cycles and the remaining operations take 1 cycle?

a) 20  

b) 25

c) 30

d) 35

e) None of the answers above is correct.

Cycles = ?
Multiple Choice

6. Itanium processor, ILP (EPIC): A vector operation \(vc = va + vb\) with 5 elements per vector shall be performed. How many cycles are required within the loop below for the vector operation above (neglect the branch operation \(br.ctop\)) if the load (\(ldl\)) instructions take two cycles and the remaining operations take 1 cycle?

a) 5
b) 9
c) 10
d) 25
e) None of the answers above is correct.

Intels’s Itanium

\[
\begin{align*}
\text{ld } r2 &= \text{addr}(va) \\
\text{ld } r3 &= \text{addr}(vb) \\
\text{ld } r4 &= \text{addr}(vc) \\
\text{ld.lc} &= 4 \\
\text{ld.ec} &= 5 \\
\text{loop:} \\
(p16) \ & \text{ldl } f32 = [r2], 8 \\
(p17) \ & \text{ldl } f36 = [r3], 8 \\
(p19) \ & \text{fadd } f38 = f35 + f38 \\
(p20) \ & \text{stl } [r4] = f39, 8 \\
& \text{br.ctop.loop} \\
\end{align*}
\]

Cycles = ?
Multiple Choice

7. Itanium processor: Which hazard can be circumvented by register rotation?
   a) Control hazards
   b) Data hazards
   c) Structural hazards
   d) None
   e) None of the answers above is correct.

8. Which MIMD systems are best scalable with respect to the number of processors?
   a) Distributed memory computers
   b) ccNUMA systems
   c) nccNUMA systems
   d) Symmetric multiprocessors
   e) None of the answers above is correct.
Multiple Choice

9. Workload driven evaluation of parallel systems, memory constrained scaling: A matrix factorization with complexity $n^3$ takes 2 hours for a square matrix which requires $8*10^8$ bytes on one processor (8 bytes per element). Which time would it need on 100 processors (ideal speedup)?
   a) 1 hour
   b) 2 hours
   c) 10 hours
   d) 20 hours
   e) None of the answers above is correct.

10. Workload driven evaluation of parallel systems, time-constrained scaling: Which should be the number of rows for a matrix-matrix multiplication on 64 processors if it is 500 on 1 processor (assuming ideal speedup)?
    a) 2000
    b) 4000
    c) 6000
    d) 8000
    e) None of the answers above is correct.
Multiple Choice

11. Interconnection networks, topology: How many links has a 5 by 5 mesh?
   a) 16
   b) 25
   c) 40
   d) 50
   e) None of the answers above is correct.

12. Interconnection networks, topology: Which is the height of a binary tree with 32 nodes?
   a) 4
   b) 5
   c) 8
   d) 16
   e) None of the answers above is correct.
13. Interconnection networks, topology: What is the difference between a 2-D torus and a hypercube with 16 nodes?
   a) None
   b) Node degree of 2-D torus is lower.
   c) Bisection bandwidth of hypercube is higher.
   d) Average distance of hypercube is significantly lower.
   e) None of the answers above is correct.

14. Interconnection networks, E-cube routing: Which is the path taken from 001 to 110?
   a) 001 -> 101 -> 111 -> 110
   b) 001 -> 000 -> 010 -> 110
   c) 001 -> 011 -> 111 -> 110
   d) 001 -> 011 -> 010 -> 110
   e) None of the answers above is correct.
15. Cache coherence: For which shared (virtual) memory systems is the snooping protocol suitable?
   a) Crossbar connected systems
   b) Systems with hypercube network
   c) Systems with butterfly network
   d) Bus based systems
   e) None of the answers above is correct.

16. Snooping cache protocol: In which case is the main memory not up-to-date?
   a) Write-through caches: After writing to shared data
   b) Write-back caches: Cache data marked as exclusive
   c) Write-back caches: Cache data marked as modified
   d) Write-back caches: Cache data marked as shared
   e) None of the answers above is correct.
17. Snooping cache protocol, write-back caches: What is an immediate effect of writing to shared data in the cache of one processor?
   a) Updating main memory
   b) Updating copies in the caches of other processors
   c) Marking copies in the caches of other processors as modified
   d) Invalidating copies in the caches of other processors
   e) None of the answers above is correct.

18. Directory-based cache coherence protocols for distributed memory systems: Which information must the directory of each processor contain?
   a) Only status information on its cache data
   b) Status information on its cache data + locations of copies
   c) Only locations of copies
   d) Status information on its cache data + locations of copies + status information on data in memory of other processors
   e) None of the answers above is correct.
Multiple Choice

19. What is the main difference between an instruction pipeline and a vector pipeline (VP)?
   a) VP: The instruction pipeline stage WB is further segmented.
   b) VP: The instruction pipeline stage ID is further segmented.
   c) VP: The instruction pipeline stage IF is further segmented.
   d) VP: The instruction pipeline stage EX is further segmented for floating point operations.
   e) None of the answers above is correct.

20. What is the start-up time in cycles for 2 vector pipes with 5 segments each if chaining is applied?
   a) 4 cycles
   b) 5 cycles
   c) 9 cycles
   d) 10 cycles
   e) None of the answers above is correct.
Multiple Choice

21. Which vector functions that are hardware supported on vector systems are not involved in the vectorization of IF blocks?
   a) Gather/scatter
   b) Vector mask
   c) Inverted vector mask
   d) Compress/expand
   e) None of the answers above is correct.

22. What is a main advantage of classical vector systems (VS) compared with RISC based systems (RS)?
   a) VS have significantly higher memory bandwidth than RS.
   b) VS have higher clock rates than RS.
   c) VS are more parallel than RS.
   d) VS have more disk space than RS.
   e) None of the answers above is correct.